MODEL QUESTION PAPER SET- 1 : 2021 - 22

MM : 70 **COMPUTER SCIENCE Paper - II (THEORY)** **Time : 3 Hrs**

SOLUTION

Entire Syllabus

Q 1 (A)

i. d) 8048
ii. a) MOV
iii. c) Repeater
iv. d) RAL

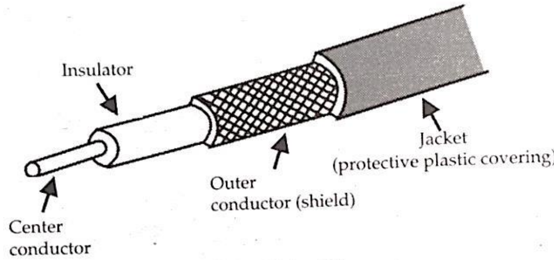
(B)

i.

no	Microprocessor	Microcontroller
1	It can read instructions and execute programs.	It can read instructions and execute programs also perform communications, perform event counting.
2	It has no on-chip Program memory.	It has on-chip program memory in the form of RAM up to some hundreds of bytes.
3	It has no on-chip Fix memory.	It has on-chip Fix memory in the form of some KB of ROM.
4	It doesn't have timer and event on the chip.	It consists of timer and event counter.

ii. **1. Stack pointer :**
It's a sixteen bit register.
It is used to store memory address of special memory called as stack memory.
When Data is stored on stack the SP decrements by two, and increments by two when data is read from stack.
2. Accumulator : It is an eight bit register.
It is used to store first operand while performing arithmetic or logical operations.
It also stores the result of the operation done in ALU.
3. ALU : It is an Arithmetic and Logical Unit.
It commonly gets inputs from Accumulator and Temporary register.
This performs arithmetic operations such as add, subtract etc and logical operations such as AND OR etc.
According to result in ALU, alg bits are set or reset.

iii. **Co-axial cable :**
It's a cable used in networking for communication i.e. for transfer of data between different computers.
Construction :
Solid copper or stranded wire at the centre.
Surrounded by plastic insulation.
Wire mesh or metallic foil covers the insulator. This Reduces the EMI
The outer plastic cover provides protection and insulation.



Co-axial cable

Features :

Can be used for long distances with high speed

Better resistance to EMI

Attenuation is less

Q. 2 (A)

i. **1. READY :** It is an input signal. Its active high.

It is connected to a slower device working with processor.

If the device is Not ready it sends zero signal to processor. In response processor goes into wait state.

When the device is ready it sends high i.e. signal 1 to processor and processor proceeds further

2. IO / M : It is an output pin.

It performs two functions.

When the processor is performing memory operations the pin outputs low i.e. 0

When the processor is performing Input/output operations it outputs high i.e. 1

3. SOD : It is Serial Output data pin. It is an output pin.

The pin is used to output one bit (1 / 0) in serial data output.

The serial data output is controlled by SIM instruction.

ii. **80286 processor:** It's a 16-bit processor.

Data bus is 16-bit.

Address bus is 24-bit.

Works on two modes : Real and Protected modes.

Can access 1GB of virtual memory.

80486 processor :

It's a 32-bit processor. Developed in 1989

32 bit Address bus.

Can access up to 4GB memory

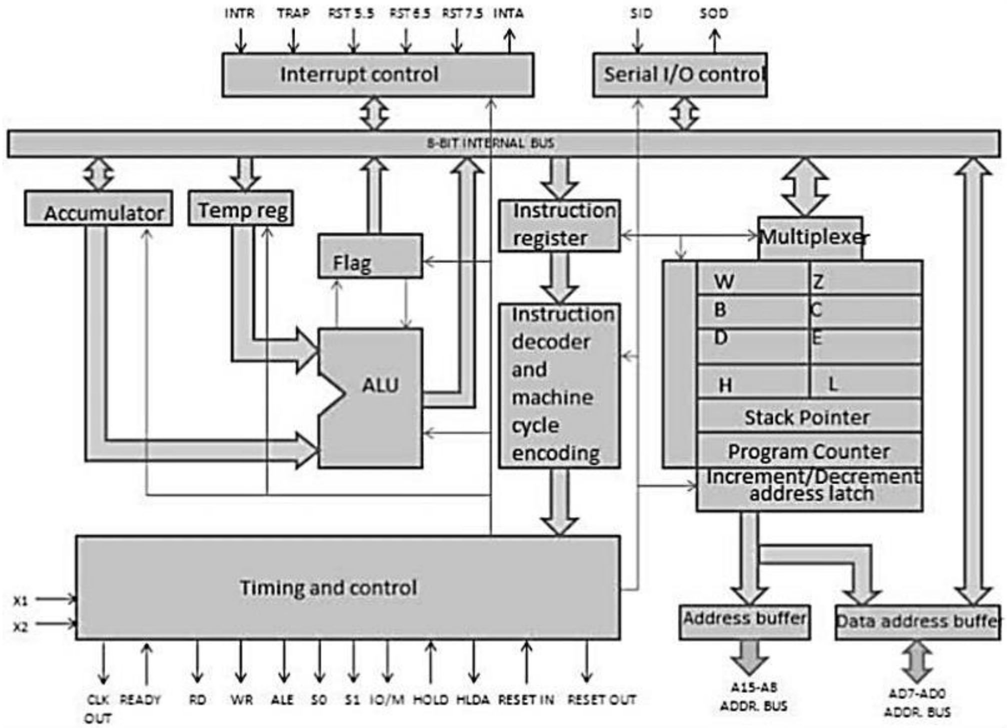
Has Math co-processor

iii. The main Features of 8051 are as listed below :

1. The 8051 microcontroller has an 8-bit ALU
2. The 8051 has 4K byte (4K × 8 bit) ROM or EPROM.
3. The 8051 has 128 byte (128 × 8 bit) RAM
4. It has dual 16-bit timer event counter.
5. It has 32 I/O lines for four 8-bit I/O ports.
6. It can address 64 kB of program memory.
7. It can address 64 kB of data memory.

Q. 2 (B)

i. Block diagram of 8085



ii. Programming model of 32-bit processors :

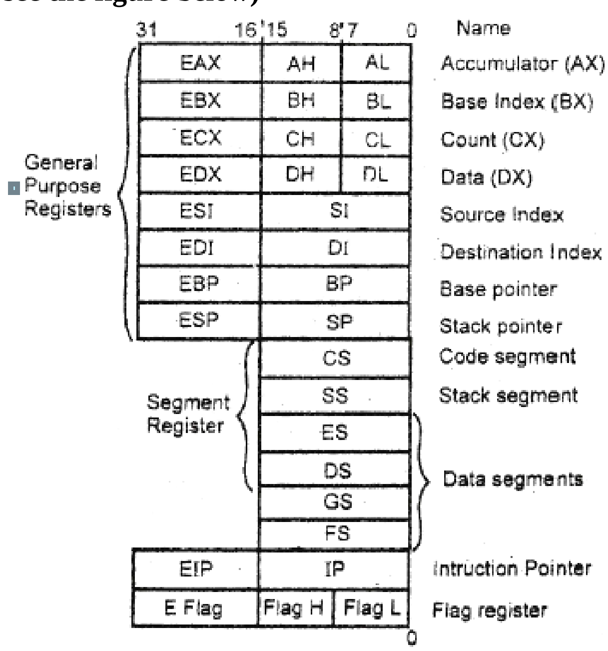
It has general purpose registers like A, B,C, D which can be used as 8bit, 16bit or 32bit registers.

Index and pointer registers like SI, SP, BP etc are used to refer to memory. These registers can be used as 16bit or 32bit registers.

Segement registers are used to store base addresses of segments and these are 16bit registers.

Flag register is 32 bit.

(see the figure below)



Q. 3 (A)

i. Addressing modes of 8085 :

Addressing mode specifies the way / format in which operands are mentioned in any instruction.

1. Direct addressing : Here the address of an operand is directly mentioned in the instruction, after the opcode. The instruction is either two bytes or three bytes.

e.g. STA 2005H

2. Immediate addressing : Here the operand is an immediate data mentioned after opcode in the instruction. One or two byte data appears after the opcode.The instruction is Two or Three byte instruction.

e.g. MVI A, 05H , LXI B, 2034H

3. Implicit addressing : Here the operand is Not mentioned in the instruction, but it is predefined operand. (operand is implied)

In Some instructions Operand is Accumulator.

One byte instructions.

e.g. CMA , SIM, STC

ii. 1. Star topology : All comp are connected to central comp.

Central comp receives data and transmits to proper destination.

Advantages:

Adding new Comp is easy.

Control is centralized.

Disadvantages:

Costly central comp required

If central comp fails, the NW is affected.

2. Bus topology :

Multiple computers connected to same cable - Backbone

Each comp. can send data to another comp. using bus.

Backbone cable carries message along the cable, as message arrives at a comp. it checks the addr If it matches it receives the message, else goes to next comp

Advantages:

Faster communication.

Easy installation.

Breakdown of one comp, wont affect other.

Used in LAN

3. Ring topology :

Each comp works as receiver and trans.

Data flows in one direction only.

Data is transmitted with addr.

Uses a token passing. The Node that currently holds a token, can transmit data

Costly wiring and adapters required.

One Comp fails, the N/W is affected.

Advantages:

Easy installation.

Each comp can transmit data, no central comp

iii. LAN / WAN

LAN (Local Area Network)	WAN (Wide Area Network)
1. Group of Computers connected in small areas	1. Group of Computers or networks connected in larger areas
2. Data transfer rate is high.	2. Data transfer rate is Not very high.
3. Generally Co-axial cables are used	3. Generally telephone cables, microwave towers, and satellites are used
4. Noise and other disturbance is less	4. Noise errors and atmospheric disturbances are possible.
5. e.g. College lab	5. e.g. internet

Q.3 (B)

i. Vectored interrupts :

An interrupt for which jump address (sub-routine address) is fixed is called as Vectored interrupt.
Microprocessor 8085 has four hardware interrupts : TRAP, TST7.5, RST6.5 and RST5.5
And eight Software interrupts (instructions) RST 00, RST 01, ... RST 07.
When any external device needs to interrupt the processor it high signal to processor on respective pin.
In response processor completes its current instruction, sends Interrupt Acknowledge signal to the device and jumps to the corresponding subroutine for the interrupt. After finishing the subroutine program returns back to main code, and continues execution of main code.
Same way when any RST n instruction works, program jumps to specific address, executes the subroutine and returns back to main code.
Jump address is given by N * 8.
e.g. when RST 03 .. instruction works program will jump to address 3*8 = 24 (i.e. 0018H) .
Also if RST 6.5 interrupt arrives then program jumps to address 6.5 * 8 = 52 (i.e. 0034H)
Priority in case of hardware interrupts, the priority of TRAP is highest and RST 5.5 is lowest.

ii. Pentium processor:

1. Dual pipelining : Processor can execute two instructions simultaneously.
This achieves very high performance.
2. Pre-fetching : Pre-fetching is loading instruction in advance, while current instruction is executed.
The pre-fetched instruction are stored in Queue and can be read by processor without delay.
3. Branch prediction : This logic predicts if any branch instruction will work.
If branching is predicted the next instruction will be loaded from branch address.
Thus, time for loading new instructions is saved and pipelines have next instruction ready.
4. Internal cache : Cache is very fast memory that is used to store some MBs of instructions and data. Internal cache serves purpose of storing the latest code so that it need not be read from external memory i.e. RAM. Reading program from memory is slower.

Q. 4 (A)

i. Protocol :

Protocol is a set of rules and formulae used by the communicating devices.
These set of rules governs how data is really transferred between the two devices.
Networks use protocols like HTTP , FTP, TCP/IP etc.

TCP/IP Protocol :

The most important and base protocol is TCP/IP (transport control protocol / Internet protocol).
Every device that performs communication over network uses this protocol
The protocol is effectively a set of rules that describe how the data is passed between the computers.
To send a data packet to another computer it establishes connection with the receiving device and then sends the packets. If packet is not received then it resends the packet.

ii. Flag register of 8086 :

8086 has 16-bit flag register.
Out of 16 bits, only 9 bits are used as Flag bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	OF	DF	IF	TF	S	Z	U	AC	U	P	U	Cy

where,
Cy – Carry flag,
P – Parity flag
AC – Auxiliary carry flag,
Z – Zero flag,
S – Sign flag,
TF – Single step trap,
IF – Interrupt flag,
DF – direction flag
OF – over flow flag

Q.4.(B)

i. **1. XCHG : Exchange.**

The instruction exchanges the contents of HL and DE register pairs.

Before XCHG :	HL	2365 H	DE	4583 H
After XCHG:	HL	4583 H	DE	2365 H

1 byte instruction
Uses implicit addressing.
No flags affected.

2. XTHL : Exchange the contents of Stack top with Reg. pair HL

before XTHL : HL 2365 H SP 4000 H → Stack A3 4F H

after XTHL : HL 4FA3 SP 4000 H → Stack 65 23 H

3. CPI : Syntax – CPI 8-bit data

Compare 8-bit value with contents of Accumulator.
After comparison flags are modified to indicate the result of comparison.
No other register or memory value is affected.
The flags change as follows :
If A > 8-bit value … carry =0 , Zero=0
If A = 8-bit value … Zero = 1
If A < 8-bit value … Carry = 1

4. RNZ : Return if Not Zero.
Program returns to main program if zero flag is Not set i.e. zero flag is zero.
The return address is picked from Stack top.
No flags affected
1 byte instruction.
Implicit addressing.

ii. Characteristics of Media :

While choosing a media for communication one has to consider following thing.

- Cost of installation.
- Installations.
- Bandwidth (data transfer capacity)
- Attenuation
- Immunity to Electromagnetic Interference (EMI)

Bandwidth :

- Measure of Capacity of medium to transmit data
- Defined as rate of bits per second (commonly in MBPS)
- Short cable – high bandwidth, Long cables – Low bandwidth

Attenuation :

- Measure of how much a signal can weaken when it travels through the medium.
- Limits length of medium , if care not taken Receiver may receive noisy data
- Repeaters are used to regenerate signals

Immunity to EMI:

- EMI through surrounding devices can disturb the signal in medium.
- Cables are shielded properly using some insulating and other material to reduce EMI.

Q.5 (A)

i. Program to multiply numbers :

Label	Instruction	Description
	LXI H, 1051H	Set memory pointer HL to 1051
	MOV C, M	Copy memory data to C (one operand)
	INX H	Increment memory pointer
	MVI B, 00H	Set B to value zero (counting carry)
	MVI A, 00H	Set Accumulator to zero (for product)
LOOP :	ADD M	Add memory value (second operand) to A
	JNC SKIP	If carry not set jump to next operations
	INR B	Increment Carry counter B
SKIP:	DCR C	Decrement counter
	INX H	Increment Pointer HL
	JNZ LOOP	If zero flag not set jump to loop
	INX H	Increment memory pointer
	MOV M, A	Store A to memory (Lower byte of result)
	INX H	Increment memory pointer
	MOV M, B	Move B to memory (Higher byte of result)
	HLT	Stop

ii. Counting multiples of 2 :

Label	Instruction	Description
	LXI H, 20A0H	Set memory pointer HL to 20A0
	MVI C , 32H	Set byte counter to 32H (i.e. 50)
	MVI B, 00H	Set B to zero (counter for multiple of 2)
LOOP :	MOV A, M	Move memory to A
	RRC	Rotate A right once
	JC SKIP	If carry set jump to SKIP (next operations)
	INR B	Increment counter B
SKIP :	INX H	Increment memory pointer H
	DCR C	Decrement byte counter C
	JNZ LOOP	Jump to loop if zero flag is not set
	MOV A, B	Move B to A (count)
	STA 3000H	Store A at address 3000H
	HLT	Stop

iii. Program to transfer block of data.

For source block : Starting address = 1021H , Ending address = 1035H

Difference = 1035 H – 1021H = 14 H

No of bytes to transfer = 14 + 1 = 15H

Label	Instruction	Description
	LXI H, 1021H	Set memory pointer HL to 1021H (for source block)
	LXI D, 2000H	Set pointer DE to 2000H (for destination block)
	MVI C , 15H	Set byte counter to 15H
LOOP :	MOV A, M	Move memory to A
	STAX D	Move A to memory address given by DE pointer
	INX H	Increment memory pointer H
	INX D	Increment memory pointer D
	DCR C	Decrement byte counter C
	JNZ LOOP	Jump to loop if zero flag is not set
	HLT	Stop

OR

Q.5 (A)

i. Adding two 2-byte numbers

Label	Instruction	Description
	MVI B, 00H	Move 0 to B. (for carry)
	LHLD 2001H	Load 2 bytes from 2001H to HL pair
	XCHG	Exchange HL with DE
	LHLD 2003H	Load 2 bytes from 2003H to HL pair
	DAD D	Add HL and DE, store result in HL
	JNC DONE	If carry not set then jump to done
	INR B	Increment B (to make 1)
DONE :	SHLD 2005H	Store HL pair (sum) to 2005H
	MOV A, B	Move B to A (Carry value)
	STA 2006H	Store A to 2006H
	HLT	Stop

ii. Results of given instructions :

Given : A= C5H , B=73H

1. CMP B :

Contents of A unchanged

Sign flag = 0

Carry flag = 0

2. ADI 32H

Contents of A = F7H

Sign flag = 1

Carry flag = 0

3. CMA

Contents of A : 0011 1010 i.e. 3AH

Sign flag = 0

Carry flag = 0

4. XRA B

Contents of A : 1011 0110 i.e. B6H

Sign flag = 1

Carry flag = 0

5. ADD B :

Contents of A :3 8H

Sign flag = 0

Carry flag = 1

iii. Counting number of times 2AH value in a memory block

Label	Instruction	Description
	LXI H, 2000H	Set memory pointer HL to 2000H
	MOV C, M	Move memory to C (length of block)
	INX H	Increment HL pointer
	MVI B, 00H	Set B to 0 (counting 2AH)
	MVI A, 2AH	Copy 2AH in A (for comparing)
LOOP:	CMP M	Compare memory with A
	JNZ SKIP	If zero flag not set , jump to skip
	INR B	Increment B
SKIP :	INX H	Increment pointer HL
	DCR C	Decrement C
	JNZ LOOP	Jump to Loop if zero flag not set
	MOV A, B	Move B to A
	STA 3001H	Store contents of A to address 3001
	HLT	Stop

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